# EXHIBIT 3

**Comparison of Netlist's Asserted Independent Claims of the '506 and '608 Patents**

| '608 Patent, Cl. 1 | '506 Patent Cl.1 & Cl. 14 | |
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| **(1pre).** A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br>**(1a)** a module board having edge connections for coupling to respective signal lines in the memory bus;<br>**(1b)** a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device **being further configured to receive a system clock signal and output a module clock signal;** and<br>**(1c)** memory devices mounted on the module board and configured **to receive the module command signals and the module clock signal,** and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and<br>**(1d1)** a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal | (1pre). A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:<br>(1a) a module board having edge connections to be coupled to respective signal lines in the memory bus;<br>(1b) a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;<br>(1c) memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals,<br>(1d) wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by **outputting read data and read strobes** associated with the memory read operation; and<br>(1e) wherein a first memory device in the selected rank is configurable **to output at least a first section of the read data and at least a first read strobe**; and<br>(1f) data buffers on the module board and coupled | (14pre). A method, comprising:<br>(14a) at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer,<br>(14b) wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;<br>(14c) receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines<br>(14d) outputting, at the module control device, registered C/A signals in response to the input C/A signals,<br>(14e) wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by **outputting read data and read strobes** associated with the memory read operation, and<br>(14f) wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to **output at least a** |

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| lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, **and configured to receive the module control signals and the module clock signal**,<br>**(1d2)** the each respective buffer circuit **including a data path corresponding to each data signal line** in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and **to control the data path in accordance with the module control signals and the module clock signal**<br>**(1d3)** wherein **the data path corresponding to the each data signal line** includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to **delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.** | between the edge connections and the memory devices,<br>(1g) wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and<br>(1h) wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals<br>(1i) **delay the first read strobe by a first predetermined amount to generate a first delayed read strobe**<br>(1j) **sample the first section of the read data using the first delayed read strobe**; and<br>(1k) transmit the first section of the read data to a first section of the data bus;<br>(1l) wherein **the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations**. | **first section of the read data and at least a first read strobe;**<br>(14g) outputting, at the module control device, module control signals<br>(14h) receiving, at each of the data buffers, the module control signals from the module control device<br>(14i) the method further comprising, at the first data buffer, in response to one or more of the module control signals<br>(14j) **delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe**<br>(14k) **sampling the first section of the read data using the first delayed read strobe**; and<br>(14l) transmitting the first section of the read data to a first section of the data bus; and<br>(14l) the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, **determining the first predetermined amount based at least on signals received by the first data buffer**. |